REMARKS

This paper is filed in reply to the action mailed October 19, 2004. The applicant asks that all claims be allowed in view of the foregoing amendments and the following remarks.

Claims 1-41 are pending in the present application. Claims 1, 15, 18, 24, 29-31 and 36 have been amended. Claim 16 has been cancelled. Claims 42-45 have been added.

1. Interview

The applicant thanks the Examiner for the interview on December 14, 2004. The Satou reference and its relevance to claim 1 was discussed. No agreement was reached.

2. Objections to Claim 15

The applicant thanks the Examiner for the suggestion that the informalities objected to in claim 15 can be corrected by changing "a processor" to "the processor" in line 5 of the claim. Claim 15 has been amended rendering the objection moot as to this claim.

3. Response to Rejections Under 35 U.S.C. 102(e)

Claims 1-6, 9, and 15-41 stand rejected under 35 U.S.C. 102(e) as being anticipated by Satou et al., U.S. Patent 6,101,584. Applicant respectfully traverses the rejection.

a. Claims 1-6, and 9

Amended claim 1 recites a method for controlling access to a dynamic random access memory (DRAM), arranged in a computer system having a processor and memory controller. The processor is controlled by a microcode instruction program. The method comprises performing, for each DRAM access, a predetermined number of DRAM control operations in response to a corresponding sequence of control instructions included in microcode instructions of the microcode instruction program. Each DRAM control operation corresponds to a

predetermined sub cycle of a DRAM access so that an entire sequence of DRAM control operations is required for a complete DRAM access.

Satou relates to a computer system that includes a memory and a CPU for making interlock access to the memory. The computer system comprises a CPU 110, a DRAM 120, a cache 130, a clock unit 140, and external bus interface 150 and a memory controller 160 as well as various bus and control interfaces. Satou discloses a memory controller that prevents the DRAM from being externally accessed while the CPU performs an interlock access.

Satou does not disclose the invention recited in claim 1. Applicant disagrees with the Examiner's assertion that a "read or write operation, such as operation code LOAD" is a DRAM control operation. Amended claim 1 recites that for each DRAM access, a sequence of DRAM control operations is performed in response to a corresponding sequence of microcode-implemented control instructions. See also Specification page 5, line 28, to page 6, line 15. This means that for a read access to the memory, a sequence of DRAM control operations has to be performed. In one embodiment of the invention, described in Table II on page 17 of the specification, a read access requires a sequence of three DRAM control operations (R, H, E) to be executed. Table I on page 14, illustrates an example of the correlation between the control instructions in the special control instruction field (MEMCP) of the microcode instructions and the corresponding DRAM control operations R, W, H, E. Each DRAM control operation generates DRAM control signals for a predetermined sub cycle of a DRAM access. Hence a single DRAM control operation, or more generally a memory control operation, does not correspond to an entire memory access such as Read/Write, but merely to a sub cycle of such an access. An entire sequence of memory control operations is required to complete a memory access. Therefore, the DRAM control operation recited in claim 1 does not correspond to a complete memory access.

The instructions for performing the read and write operations in Satou are not microcode instructions. A person of ordinary skill in the art would understand that the instructions in Satou are machine code instructions and not microcode instructions. Microcode instructions are understood by one of ordinary skill as instructions performing specific processing functions that

are fixed in storage that is not program addressable. The dictionary meaning of microcode instructions is "Very low-level code, even lower in level than machine code, [that] specifies what the processor does when it executes a machine code instruction." Microsoft Computer Dictionary, Fourth Edition, page 289 (Copyright 1999). It is well-known to the skilled person that microcode is not an application program loaded into the CPU from DRAM, but rather the microcode is part of the CPU and resides in a dedicated control store within the CPU responsible for the CPU control. The microcode is in general completely unknown to the application programmer.

Satou does not disclose the implementation of a DRAM access using a sequence of microcode-implemented control instructions as recited in claim 1. Applicant's specification describes a CPU controlled by a processor control unit 20 that is implemented using a microprogram 22. See Fig. 1 and page 9, lines 1-5. In Satou, instructions of an application program are loaded one by one from DRAM into the instruction queue, where they await decoding by the instruction decoder. The CPU control components, including the CPU control unit 110j and the instruction decoder 110b, are apparently implemented in hardware. A person of ordinary skill in the art will appreciate that the instructions fetched from the DRAM into the instruction queue 110a are machine code instructions and not microcode instructions. In Satou the machine code instructions are implemented by the CPU control unit 110j and the instruction decoder 110b.

In the system of Satou, the memory controller receives a single request REQF for instruction fetch access or a request REQO for operand data access from the CPU, together with corresponding memory address signals AF and AO, respectively (col. 7, lines 55-66). For each memory access (read/write), a single general request signal, such as a request REQF for fetching instructions into the CPU from the memory system, is sent to the memory controller 160, which in turn generates a control signal CTRLD to the DRAM. Hence, in order to effectuate a single memory access, only a single request signal is sent from the CPU. This is a natural consequence of the fact that the CPU of Satou does not know in advance if the requested data/instruction will

be accessed from the cache or from the DRAM, since the computer system of Satou employs a cache memory.

In the invention recited in claim 1, for each memory (e.g., DRAM) access, an entire sequence of DRAM control instructions is transferred from the microcode instructions of the micro program 22 to the memory controller for performing a corresponding sequence of DRAM control operations (e.g. R, H, E). Specification page 14, lines 11-18 and Table I. Each DRAM control operation typically generates a single DRAM control signal, e.g., WE, CAS, RAS and COL, that corresponds to a specific sub cycle of a DRAM access.

The reference "Computer Architecture – Single and Parallel Systems" by Zargham ("Zargham") merely discloses an architecture corresponding to that of the Satou patent. There is a CPU control unit, implemented as a PLA array (not a microcode program) Fig. 2.5. An application program that adds two numbers stored in memory is loaded into memory. Program instructions of the application program are then fetched one-by-one from memory into the internal register of the CPU control unit for decoding and subsequent execution. Pages 24, 25, and Fig. 2.7. As mentioned, the CPU control unit is however not implemented by microcode. If the decoded instruction is a LOAD instruction, the memory content is retrieved from the relevant memory location. Consequently, execution of a single decoded program instruction triggers a simple read access. Page 26, Fig. 2.8. Zargham does not disclose implementing a memory access using a sequence of microcode-implemented control instructions that triggers a corresponding sequence of DRAM control operations as recited in claim 1.

Because Satou fails to disclose at least these limitations of claim 1, the reference cannot anticipate that claim. For at least these reasons, claim 1 is allowable over Satou. Claims 2-6, 9 depend either directly or indirectly from claim 1 and are therefore allowable for at least the same reasons.

b. Claims 15-23

Amended claim 15 recites a controller for a dynamic random access memory (DRAM), in a computer system having a processor. The DRAM controller is responsive to a sequence of

control instructions for controlling access to the DRAM, where each control instruction is included in a microcode instruction of a processor.

Claim 15 is allowable over Satou for at least the same reasons as claim 1. Claims 16-23 depend either directly or indirectly from claim 15 and are therefore allowable for at least the same reasons.

c. Claims 24-28

Amended claim 24 recites a computer system having a processor controlled by a microcode instruction program, a primary memory cooperating with the processor, and a memory controller for the primary memory. The microcode program includes microcode instructions having a special control instruction field holding a control instruction for memory access control. For each memory access, the memory controller executes a sequence of memory control operations in response to a corresponding sequence of control operations from the processor. Each memory control operation corresponds to a predetermined sub cycle of a memory access, and a complete sequence of memory control operations is required to implement a memory access.

Claim 24 is allowable over Satou for at least the same reasons as claim 1. Claims 26-28 depend either directly or indirectly from claim 24 and are therefore allowable for at least the same reasons.

d. Claims 29-35

Amended claim 29 recites a method for performing a virtual direct memory access (DMA) to a memory in a computer system. The method comprises storing data from/to a peripheral input/output device in a buffer, transferring the data between the buffer and the primary memory via internal paths of a processor of the computer system, where the data transfer is controlled by a microcode instruction program of the processor. For each access to the primary memory, a sequence of memory control operations is executed in response to a corresponding sequence of microcode control instructions. Each memory control operation

corresponds to a predetermined sub cycle of a memory access. An entire sequence of memory control operations is required for a complete memory access.

Claim 29 is allowable over Satou for at least the same reasons as claim 1. In addition, claim 29 is allowable over Satou for at least the following additional reasons. The Examiner interprets the buffer of claims 29 and 36 as the internal register 110d of the CPU in Satou. The DMA buffer recited in claim 29 is used by peripheral input/output devices to store data, whereas the register 110d of Satou is occupied with data required for the CPU's execution of instructions. Satou does not disclose a buffer for storing data from/to an input/output device because the content of the register 110d in Satou must be kept intact during a DMA transfer and can consequently not be used for storing data to/from any input/output devices. The Examiner also interprets the microcode program recited in the claim for controlling the data transfer between the DMA buffer and the primary memory as the instruction queue 110a. The instruction queue 110a is a prefetch buffer that stores higher-level machine instructions in turn for execution by the CPU. As previously explained, there is no mention or suggestion whatsoever of any microcode instruction program in the Satou patent.

Claims 30-35 depend either directly or indirectly from claim 15 and are therefore allowable for at least the same reasons.

e. Claims 36-41

Amended claim 36 recites a computer system having a processor and a primary memory coupled to the processor. The computer system comprises a buffer for storing data from an input/output device or to an input/output device, and means for transferring data between the buffer and the primary memory via internal paths of the processor under the control of a microcode instruction program in the processor. For each access to the primary memory, a sequence of memory control operations is executed in response to a corresponding sequence of microcode control instructions. Each memory control operation corresponds to a predetermined sub cycle of a memory access. An entire sequence of memory control operations is required for a complete memory access.

Claim 36 is allowable over Satou for at least the same reasons as claim 29. Claims 37-41 depend either directly or indirectly from claim 36 and are therefore allowable for at least the same reasons

4. Claims 7, 8, and 10-14

Claims 7, 8, and 10-14 are objected to as being dependent upon a rejected base claim. Applicant thanks the Examiner for indicating that these claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 7, 8, and 10-14 depend directly or indirectly from claim 1. Applicant respectfully submits that these claims are allowable in view of the amendments to claim 1.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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